5-day Workshop: 01st – 05th July 2024

Introduction to FPGA: Hands-On with Intel development board DE2i-150 using Quartus & ModelSim

REPORT

The Electronics & Communication Engineering Department at Lingaya's Vidyapeeth organized a five-day online workshop from 1/7/2024 to 5/7/2024, with the following day (6/7/2024) for an online assessment test as part of the Value-Added Courses (VAC).

The main objective of this workshop was to introduce the delegates to Programming of FPGAs in Verilog and to get hands-on with Quartus II, an EDA Tool, and an FPGA: Intel development board DE2i-150, thus, promoting research in the VLSI domain. The event was attended by delegates from both universities and Industries, around 41 delegates registered for this workshop.

The sessions were delivered by experts from Lingaya's Vidyapeeth: Dr. Javalkar Dinesh Kumar (HoD, ECE) Dr. Namrata Bansal (Assistant professor, ECE), and Mr. Jayaraj V S (Assistant Professor, ECE).

Day 1:

***Session1*:** Session began with an introductory talk by Dr. Javalkar Dinesh Kumar on "Introduction to FPGAs". During his delivery, he introduced FPGAs and then compared various programmable devices, namely, CPLDs, ASICs and FPGAs. He concluded the talk by emphasizing the importance of gaining knowledge in the field of programming FPGAs and their scope in Industries.

***Session 2*:** Mr. Jayaraj V S introduced the participants to the Electronic Design Automation Tool to be used during the Workshop, i.e., Quartus II by Altera, now Intel. He described the steps to follow for software installation and to procure free license from Intel (required for running all modules of the software). Later in the session, he also introduced the participants to the "Basics of programming in Verilog".

Day 2:

***Session 1*:** Dr. Namrata Bansal introduced the participants to the various modeling schemes in digital system designing. She demonstrated these schemes by writing Verilog Codes for the electronic design building blocks – logic gates. During her presentation, she verified the functionality of the codes using ModelSim simulation software using 'Forced' inputs, and concluded by introducing the need for Test Benches to verify the design functionality.

***Session 2*:** Mr. Jayaraj V S introduced the concept of Modular Programming and the need for it. He supported this concept by giving a few design examples, showing how modular programming can be useful in building neat codes.

Day 3:

***Session 1*:** Dr. Namrata Bansal built upon the previous session on modular programming, and demonstrated how to design various combinational logics in Verilog. She introduced the working and coding of *MUX 2:1* and went on to design basic logic gates and *4:1 mux* using *MUX 2:1*.

***Session 2*:** Mr. Jayaraj V S introduced the FPGA board – *Intel Altera DE2i-150,* to the delegates. He presented the *Pin Planning* concepts and pin assignment procedure required to program the FPGA board using the Verilog codes, allowing access to the switches, Red and Green LEDs, the 7-segment displays and inbuilt clock-circuitry.

Day 4:

***Session 1*:** Moving on to sequential circuits, Dr. Namrata Bansal demonstrated the working of various Flip-Flops and how to behavior code them in Verilog; she showcased how to code various designs from their Truth tables using SR, D, JK and T Flip-flops as examples.

***Session 2*:** Mr. Jayaraj V S demonstrated the working of Counters, writing the Codes for a Ring counter and Johnson Up/Down counters.

In both sessions (and henceforth), the FPGA board was programmed for each digital design and used to verify their functionality. The clock-timing difference was exhibited through these codes.

Day 5:

***Session 1*:** Dr. Namrata Bansal explained the working of complex structures like 4 Bit Asynchronous Up/counters and 4 Bit Synchronous Up/counters, and wrote their codes using T Flip-flop and other basic logic gates.

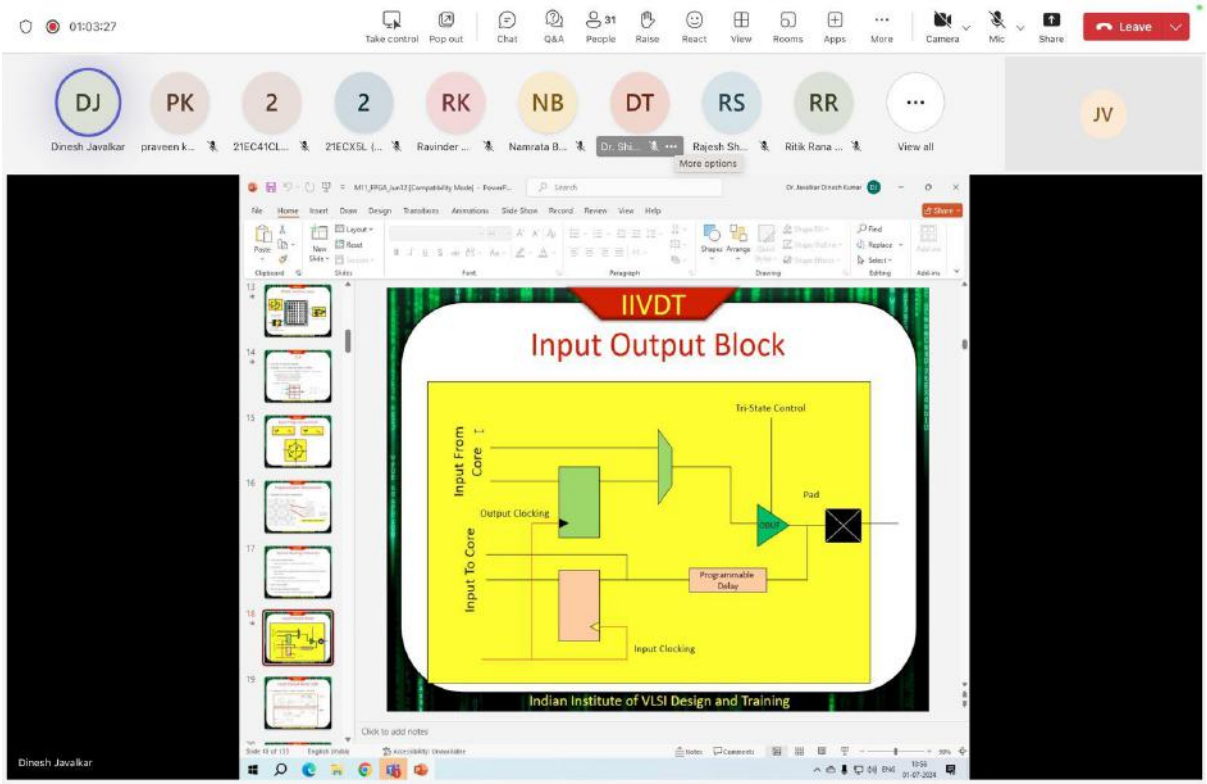
***Session 2*:** Ramping up the complexity of designs, Mr. Jayaraj V S demonstrated the working and coding of a 2x1 Vedic multiplier. Later in the session, he introduced the concept of FSMs and wrote the code demonstrating Mealy 1010 sequence detector and Moore 1010 sequence detector.

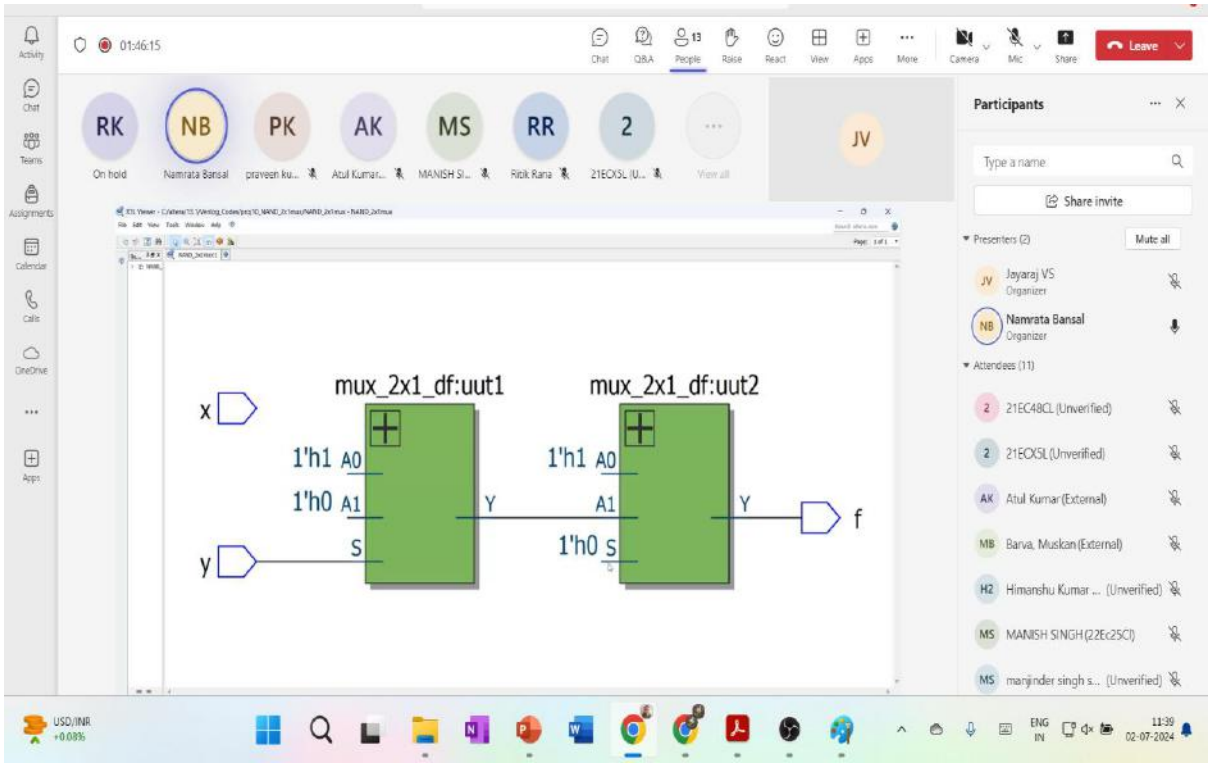
Day 6:

An online quiz comprising of questions covering the entire discussed topics was conducted through Google forms. The smooth conduction of this exam was possible due to smooth co-operation of Mr. Deepak Kumar (IT department).

The Online Workshop was conducted using the Microsoft Teams Platform, and the recording of all sessions were made available to the participants.

Workshop Screen shots and Pictures

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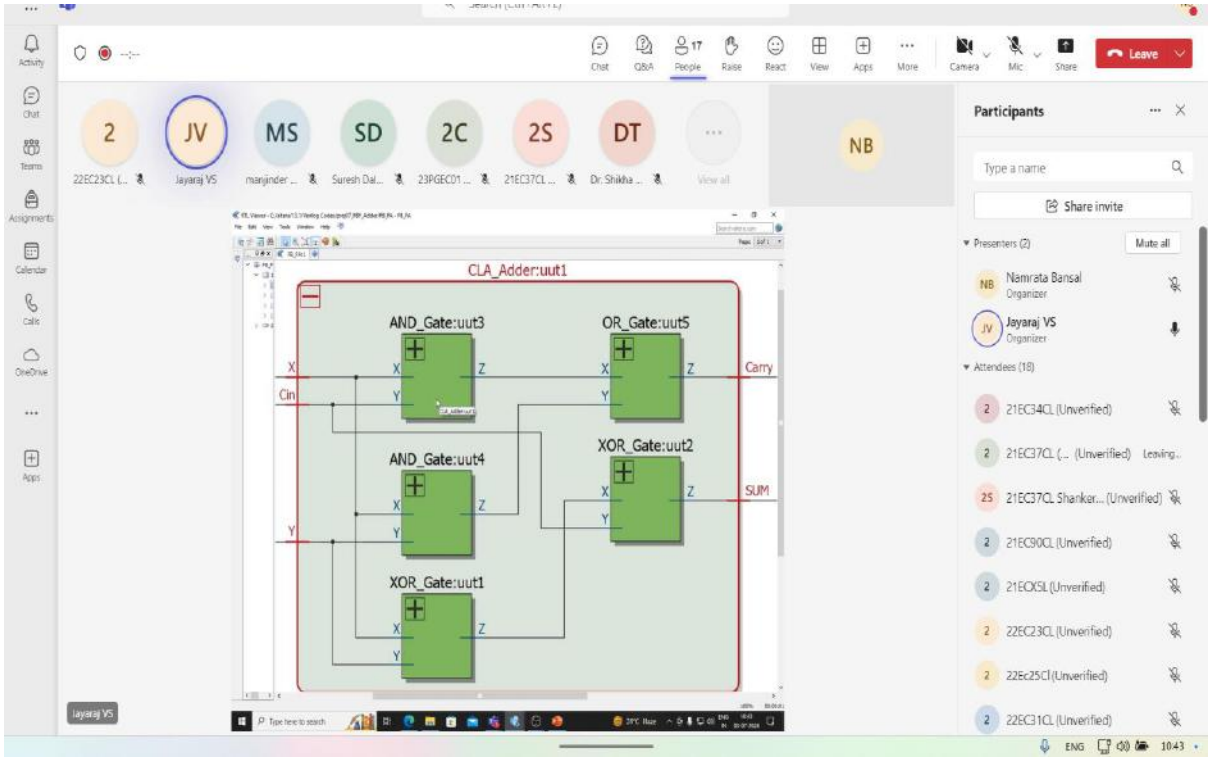
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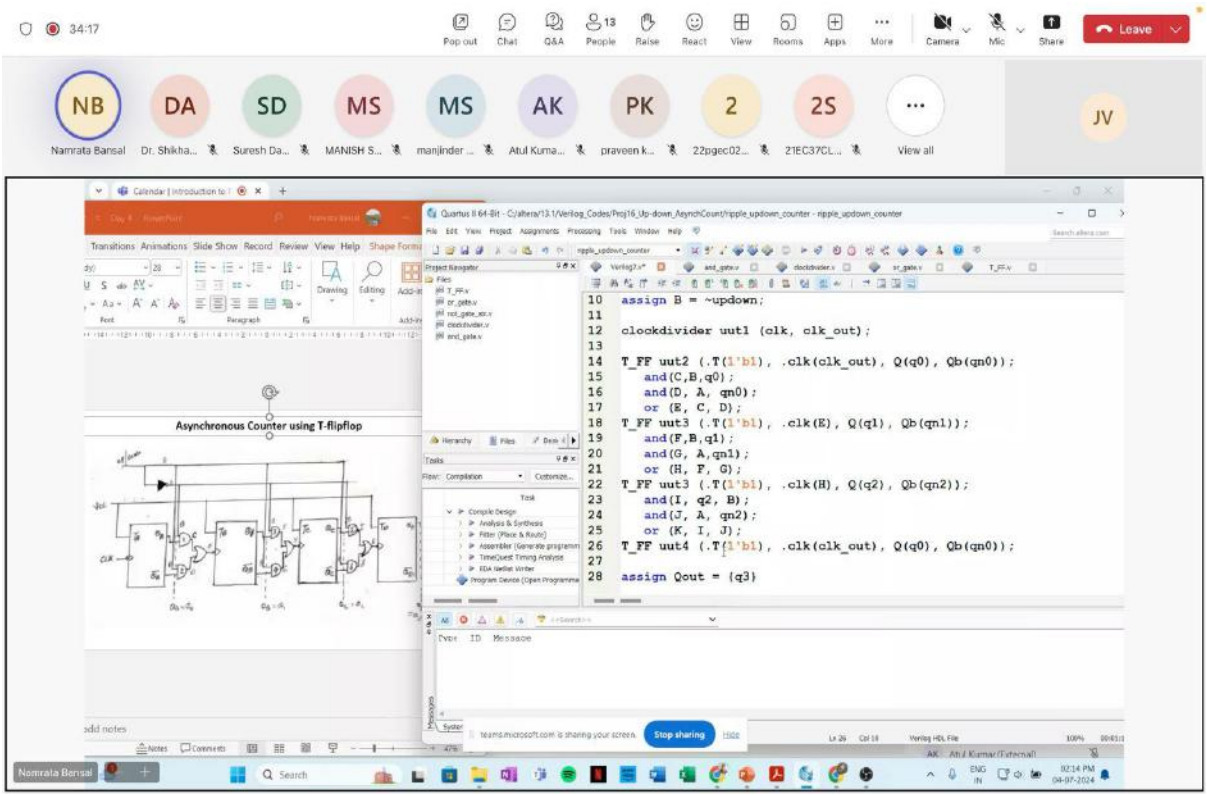
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Asynchronous Counter using T-flipflop
assign B = ~updown;
clockdivider uut1 (clk, clk_out);
T_FF uut2 (.T(1'b1), .clk(clk_out), Q(q0), Qb(qn0));
and(C,B,q0);
and(D, A, qn0);
or (E, C, D);
T_FF uut3 (.T(1'b1), .clk(E), Q(q1), Qb(qn1));
and(F,B,q1);
and(G, A,qn1);
or (H, F, G);
T_FF uut3 (.T(1'b1), .clk(H), Q(q2), Qb(qn2));
and(I, q2, B);
and(J, A, qn2);
or (K, I, J);
T_FF uut4 (.T(1'b1), .clk(clk_out), Q(q0), Qb(qn0));
assign Qout = {q3}
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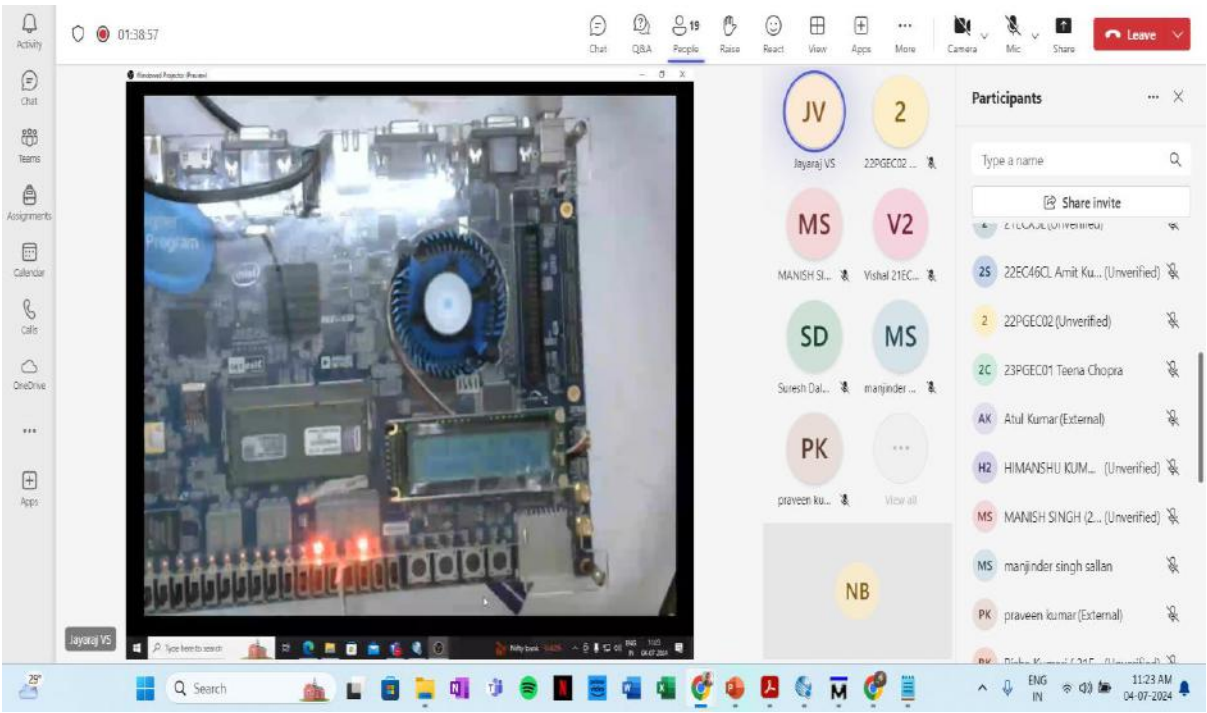
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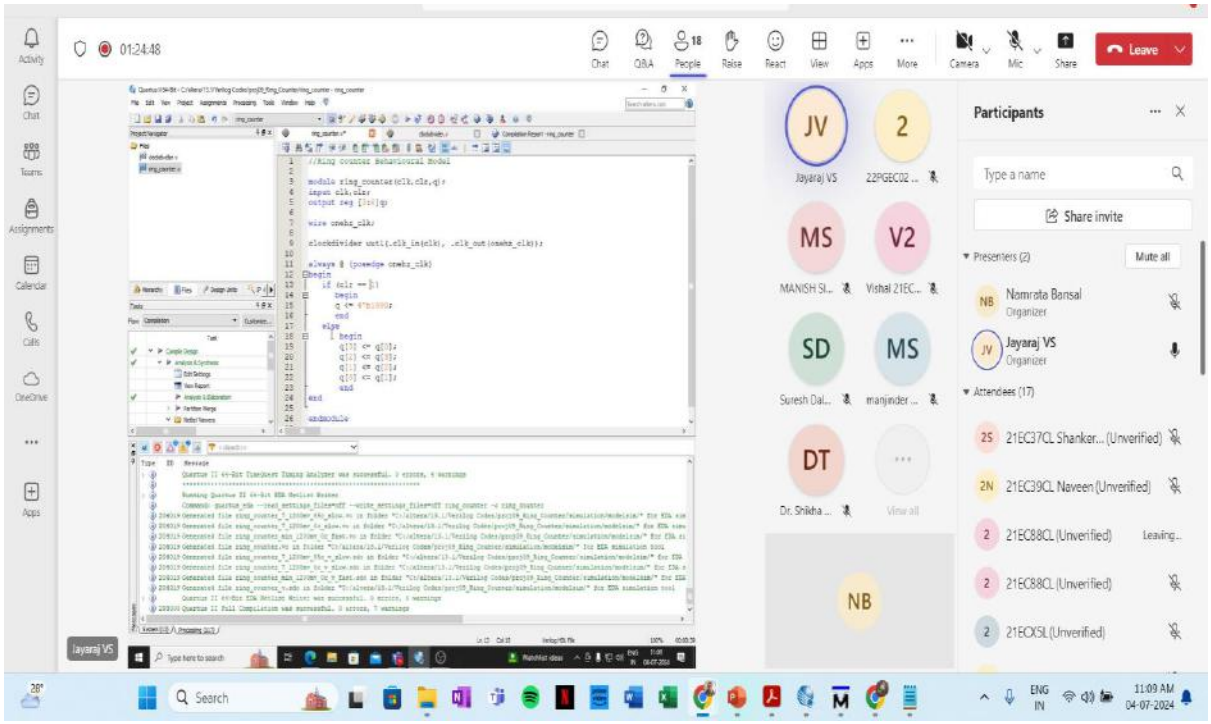
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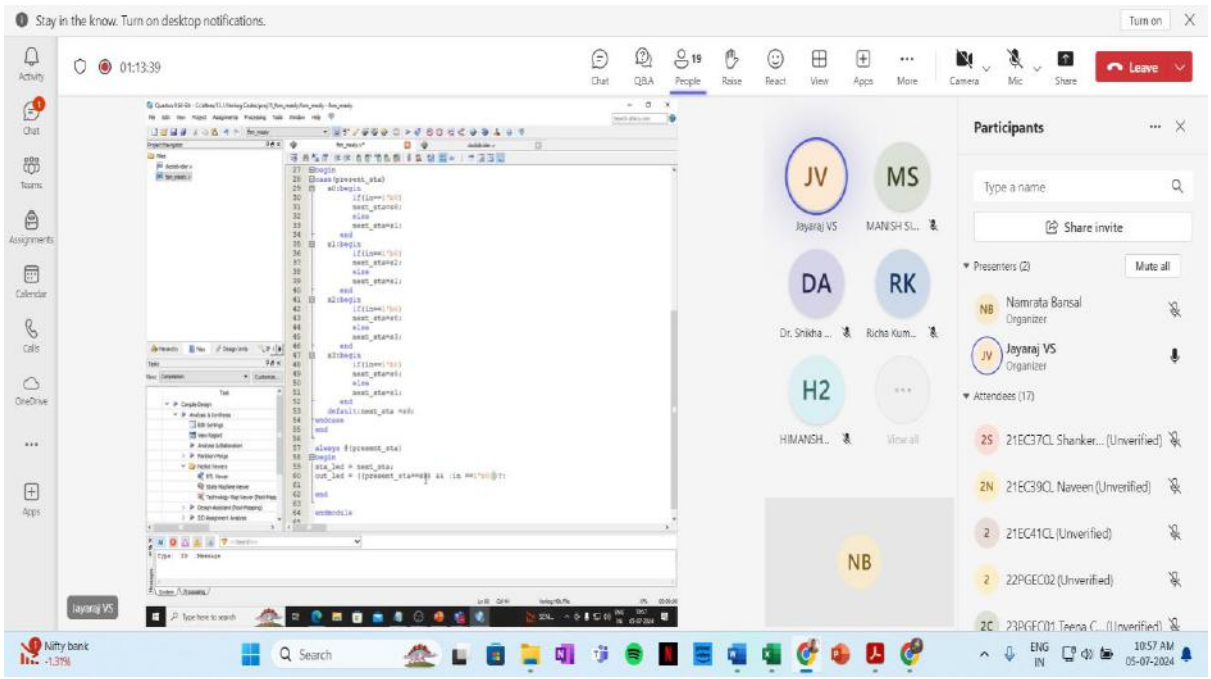
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